## PATENT APPLICATION

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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE 10 9-01

In re the Application of

Hiroji AGA, Naoto TATE, Susumu KUWABARA, Kiyoshi MITANI

Application No.: U.S. National Stage

of PCT/JP00/07111

Filed: June 11, 2001

Docket No.: 109725

For: METHOD FOR PRODUCING SOI WAFER AND SOI WAFER

### **PRELIMINARY AMENDMENT**

Director of the U.S. Patent and Trademark Office Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

#### IN THE CLAIMS:

Please replace claim 6 as follows:

6. (Amended) An SOI wafer produced by the method according to Claim 1, which has an RMS value of 0.5 nm or less concerning surface roughness for both of 1  $\mu$ m square and 10  $\mu$ m square.

## Please add new claims 7-9 as follows:

-- 7. An SOI wafer produced by the method according to Claim 2, which has an RMS value of 0.5 nm or less concerning surface roughness for both of 1  $\mu$ m square and 10  $\mu$ m square. --

-- 8. An SOI wafer produced by the method according to Claim 3, which has an RMS value of 0.5 nm or less concerning surface roughness for both of 1  $\mu$ m square and 10  $\mu$ m square. --

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